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LETTER

Bipolar Scan Waveform for Fast Address in AC Plasma Display Panel*

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SUMMARY A new bipolar scan waveform is proposed to increase the light emission duty factor by achieving the fast address in AC plasma display panel (AC-PDP). The new bipolar scan waveform consists of two-step scan pulse, which can separate the address discharge mode into two different discharge modes: a space charge generation mode and a wall charge accumulation mode. By adopting the new bipolar scan waveform, the light emission duty factor is increased considerably under the single scan ADS driving scheme due to the reduction of address time per single subfield.

key words: *plasma display panel, light emission duty factor, address time reduction, bipolar scan waveform*

1. Introduction

The ADS (Address Display Separated) driving scheme, even if used most commonly, has the low light emission duty factor problem due to the long total address time [1]. As the resolution of PDP gets higher, this problem gets more serious. Although the well-known visual problems of PDP can be lessened by using more several subfields [2], this solution also makes the light emission duty factor smaller. Therefore, the fast address technique is the most important issue for the realization of a high resolution PDP with high-class image quality. There have been many efforts to increase the light emission duty factor by reducing an address time using the various methods, such as the AwD (Address while Display) driving scheme [3], the MAoD II driving scheme [4], the partial line doubling method [1], and the plural screens method [5]. However, these methods have several weak points such as the instability in driving, the requirement of additional driving circuits, and the image quality degradation, so that more improvement is still needed.

In this letter, a new address waveform using the bipolar scan waveform is proposed to increase the light emission duty factor without any side effects mentioned above. The bipolar scan waveform uses the two-step scan pulse with two voltage polarities, which can separate the conventional address discharge into two different discharge modes: a space charge generation mode and a wall charge accumulation mode.

2. Conventional Address Scheme

In general, an address discharge in PDP means that the cells to display images are selected out prior to displaying images by accumulating the wall charges after firing the cells according to the image data from the address driver. As shown in the conventional address waveform and the related IR waveform of Fig. 1(a), the address discharge was produced between the scan (Y) and address (A) electrodes by simultaneous application of a falling scan pulse with a voltage drop of V_S and a rising address pulse with a voltage rise of V_A. For the successful address procedure, the address discharge should play two roles as follows: one is to generate the space charges for wall charges in the selected cell by simultaneous application of the scan (Y) and address (A) pulses, and the other is to accumulate the wall charges under the scan (Y) and sustain (X) electrodes by using the space charges produced from the address discharge for the ensuing sustain discharge. In the conventional address scheme, it is thought that the space charge generation for wall charges is inseparable from the wall charge accumulation during an address discharge. Accordingly, it is often thought that the scan and address pulses should have the same pulse width.

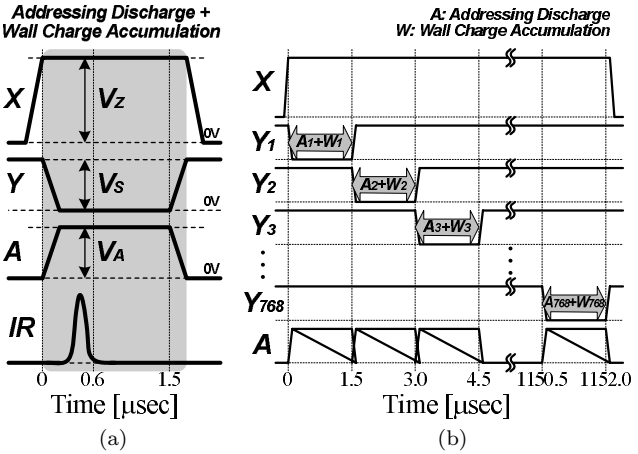

Fig. 1 Voltage and IR waveforms during single line scanning (a) and address sequence during address-period (b) in case of adopting conventional address scheme in XGA grade PDP.

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As shown in the IR waveform Fig. 1(a), the address discharge was started at 0.3 μs and extinguished at 0.6 μs after the starting point of the scan and address pulses. However, the sufficient wall charge accumulation from the space charges by the gap voltage (V_Z) between the sustain (X) and scan (Y) electrodes takes over 1.5 μs, which means that the wall charge accumulation needs a longer time than the space charge generation. Figure 1(b) shows the address sequence during an address-period in XGA grade (1024 × 768 pixels) PDP according to the conventional address scheme. The address sequence was executed line by line from the first (Y_1) to the last (Y_{768}) scan line. Each scan line must be scanned independently to avoid the misfiring problem, as shown in Fig. 1(b). The total address time depends on how long the address pulses stay on the address electrode per scan line. Thus, the total address time is determined by the address pulse width multiplied by the number of horizontal resolution of PDP. If we assume a XGA grade PDP using 8 subfields and 300 μs setup period per one subfield, the total address time per one subfield is 1152 μs and the light-emission duty factor is just 30% for a TV-field.

3. Proposed Address Scheme Using Bipolar Scan Waveform

Based on a new concept that the space charge generation can be separated from the wall charge accumulation during an address discharge, the bipolar scan waveform employed in the current research is introduced in Fig. 2(a). The new scan waveform in Fig. 2(a) has two-step scan pulse with two voltage polarities: a negative voltage polarity for producing an address discharge and a positive voltage polarity for accumulating wall charges. In the new address scheme using the bipolar scan waveform, the voltage and IR (infrared: 828 nm) waveforms applied to the three electrodes (X, Y, and A) during a single line scanning are shown in Fig. 2(a). The first address discharge, hereafter called "primary address discharge," was produced within 0.6 μs between the scan (Y) and address (A) electrodes by simultaneous application of a falling scan pulse with a negative voltage of $-V_S$ and a rising address pulse with a positive voltage of V_A at the time of T_2. After applying the negative scan and the positive address pulses for 0.6 μs, a reverse scan pulse with a positive voltage of V_R was applied to produce the additional address discharge, hereafter called "secondary address discharge," at the time of T_4. The secondary address discharge was produced between the scan (Y) and sustain (X) electrodes due to a gap voltage of V_{YX} (=V_R+V_Z). Note that this secondary address can be produced even at low gap voltage due to the presence of the space charges remaining still after the primary address discharge. Accordingly, the secondary address discharge was produced only in the cells where the primary address discharge had been produced. The reverse scan pulse width greater than 1.5 μs can accumulate the sufficient wall charges for the subsequent sustain discharges.

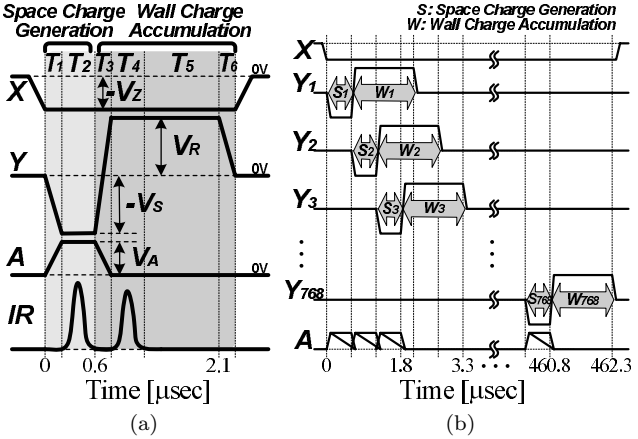

Fig. 2 Voltage and IR waveforms during single line scanning (a) and address sequence during address-period (b) in case of adopting new address scheme in XGA grade PDP.

Figure 2(b) shows the address procedure during an address-period in XGA grade PDP in the case of adopting the new address scheme. For the bipolar scan waveform, the negative pulse part was not overlapped with any other address pulse, whereas the reverse pulse part was overlapped with another address pulse. However, since the voltage polarity of the reverse pulse part was the same as that of the address pulse, no misfiring discharge was observed at the overlapping situation on condition that the voltage increase slope in the transition from the negative pulse into the reverse pulse was properly controlled. In this letter, when the transition time from the negative pulse into the reverse pulse was 300 ns, a misfiring dischage was produced. On the other hand, no misgiring discharge was produced when the transition time from the negative pulse into the reverse pulse was changed from 300 ns to 700 ns. This indicates that the misfiring problem in the bipolar scan waveform is related very closely to the voltage increase slope in the transition from the negative pulse into the reverse pulse. This problem needs to be further studied. For the transition time of 700 ns in the bipolar scan waveform, the other stable operating conditions are as follows: $-V_S = -150 - -170$ V at $V_A = 80$ V and $V_R = 140$ V or $V_R = 80 - 140$ V at $V_A = 80$ V and $-V_S = -160$ V. As a result, the address time for a single scan line can be reduced to just 0.6 μs without any undesired address discharge, as shown in Fig. 2(b). If we assume a XGA grade PDP using 8 subfields and 300 μs setup period per one subfield, the total address time per one subfield is 462.3 μs and the light-emission duty factor is increased to 63% for a TV-field.

4. Experimental Results

The 4-in. test panel with a gas mixture of Ne + Xe(4%) and a pressure of 400 Torr was employed to measure the address discharge characteristics in the case of adopting the bipolar scan waveform, and its structure and dimensions were the same as the conventional 42-in. wide VGA grade PDP with a cell pitch of 360 μm. The size of the active area was 75.60 mm × 47.52 mm. The total number of the displaying cells was 70 × 44 pixels. In this experiment, in order to examine the validity of the proposed bipolar scan waveform, the special reset waveforms, which consisted of a pair of narrow pulses and another pair of ramp-pulses with a voltage of 180 V, were used to erase only the accumulated wall charges within the cells prior to the address discharge for the purpose of minimizing the effects of wall and space charges generated from the reset discharge. As a result of adopting the special reset waveform prior to an address discharge, the minimized priming effect led to a fast primary address discharge ($< 0.6\,\mu$s) simply by raising the amplitude of the address pulse. As for the bipolar scan waveform, its voltage levels were determined based on the firing threshold voltage characteristics. In the case of 4-in. test panel employed in the current study, the firing threshold voltages between the three electrodes were observed to be 230 V for V_{XY} and V_{YX} (between two sustain electrodes), 170 V for V_{AX} and V_{AY} (A: anode, X or Y: cathode), and 250 V for V_{XA} and V_{YA} (X or Y: anode, A: cathode). From these data, the voltages were determined to be -160 V for $-V_S$, 140 V for V_R, 80 V for V_A, and -80 V for $-V_Z$, respectively. The width of the address pulse was the same as that of the negative scan pulse, and their values were 0.6 μs, whereas the width of the reverse scan pulse was 1.5 μs. These bipolar scan pulse conditions satisfy that the on-off state of the cells is exactly decided by the application of address pulse without a misfiring discharge. The address discharge characteristics were measured according to the changes in the negative scan voltage ($-V_S$) and reverse scan voltage (V_R). Figure 3 shows the dependence of the primary and secondary address discharges on the negative scan voltage ($-V_S$). Other conditions of the bipolar scan waveform are the same as those listed above. If the negative scan voltage ($-V_S$) was below -150 V, the primary address discharge was not strong enough to induce a stable secondary address discharge. On the other hands, the negative scan pulse voltage ($-V_S$) greater than -170 V could produce a weak primary address discharge without any application of address pulse, implying that undesired sustain discharges would be induced. Accordingly, the stable operation range of the negative scan voltage ($-V_S$) was determined from -150 V to -170 V. As shown in Fig. 3, in proportion as the negative scan pulse voltage ($-V_S$) increased from -150 V to -170 V, both the primary and second address discharges were initiated fast and their discharge intensities became stronger. The IR intensity of Fig. 3 shows that the stable and strong secondary address discharge can be obtained provided the primary address discharge can generate the larger amount of space charges.

Figure 4 illustrates the dependence of secondary address and ensuing sustain discharges on the reverse scan voltage (V_R) where the negative scan voltage ($-V_S$) is fixed at -160 V. Although the space charges were generated sufficiently during a primary address discharge, the reverse scan voltage (V_R) less than 80 V could not produce a strong secondary address discharge, so that the wall charges could not be accumulated sufficiently for the stable sustain discharges. On the other hand, the reverse scan voltage (V_R) greater than 140 V could induce a secondary address discharge regardless of the existence of a primary address discharge. Thus, the stable operation range of the reverse scan voltage (V_R) was determined from 80 V to 140 V. As shown in Fig. 4(a), the higher reverse scan voltage (V_R) produced the stronger secondary address

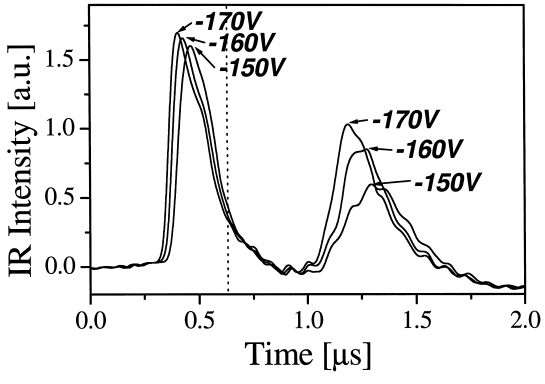

Fig. 3 Dependence of primary and secondary address discharges on negative scan pulse voltage ($-V_S$).

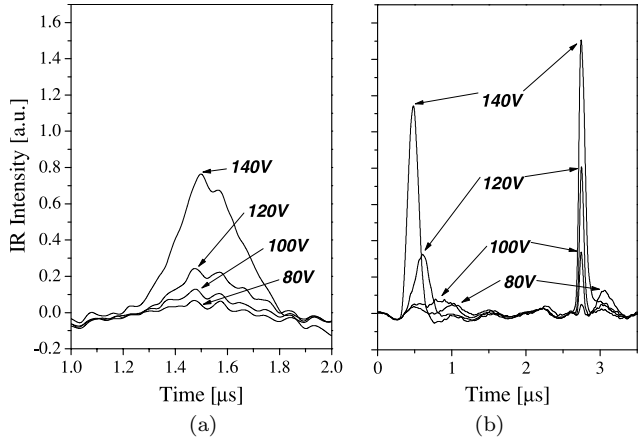

Fig. 4 Dependence of secondary address (a) and ensuing sustain (b) discharges on reverse scan pulse voltage (V_R).

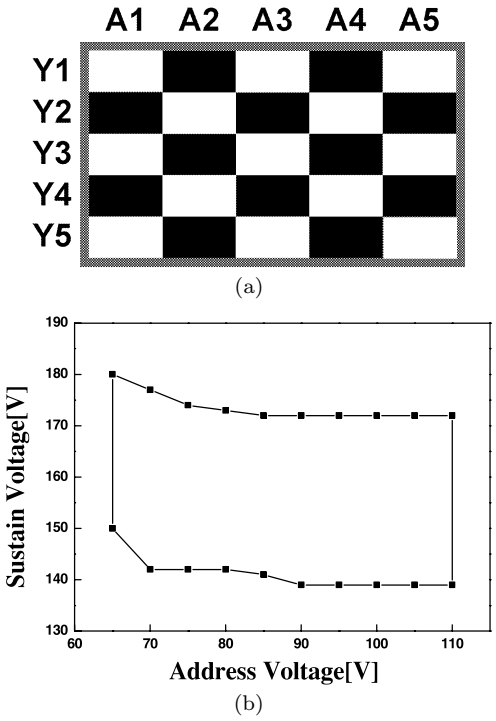

Fig. 5 Dynamic voltage margin (b) measured from checkered pattern (a) of 4-inch test panel.

discharge, thereby resulting in accumulating more wall charges below the sustain (X) and scan (Y) electrodes. Consequently, the subsequent sustain discharges also got more stable at the reverse scan voltage of 140 V.

Figure 5 shows the dynamic votage margin (b) between the address and sustain voltages measured from the checkered pattern (a) of the 4-in. test panel. The checkered pattern of Fig. 5(a) consisted of 5×5 squares to display the white and black images alternately. In the checkered pattern, the white square means the on-cells that are composed of 42×8 cells, whereas the black square means the off-cells that are composed of 42×8 cells. To check a misfiring discharge between adjacent cells, the white square was surrounded by the black square and vice versa. As a result of measuring the dynamic voltage margin under the checkered pattern displayed by the stable bipolar scan pulse conditions such as the negative scan voltage, $-V_S$ of -165 V, the reverse scan voltage, V_R of 140 V for 3 μs, and the address pulse width of 0.7 μs, the stable margin for the address voltage, V_A was obtained over 65 V,whereas the address discharge was not produced below the V_A of 65 V.

By adopting the new bipolar scan waveform during an address-period, the scanning time for a single scan line was reduced from 1.5 μs to 0.6 μs, so that the address time for single subfield at XGA grade PDP was reduced from 1152 μs to 462.3 μs, as shown in Figs. 1(b) and 2 (b). As a result, the light emission duty factor was improved up to 63% if the subfields of the XGA grade PDP were 8, and the reset period was 300 μs per single subfield. This considerable improvement of a light emission duty factor can contribute to the accomplishment of high luminance, high resolution, and high-class image quality in the PDP.

5. Conclusion

A new bipolar scan waveform was proposed for the fast address in AC-PDP. The new bipolar scan waveform could reduce the scanning time per single scan line from 1.5 μs to 0.6 μs by separating the address discharge mode into the two different discharge modes: a space charge generation mode and a wall charge accumulation mode. When compared with the conventional addressing waveform in the single scan ADS driving scheme at XGA grade PDP, the bipolar scan waveform could reduce the total address time per single subfield by about 50%, thereby achieving about two times improvement in the light emission time for a TV-field.

References

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